LOGIC Emulation Source

Daughtercard Interface Description

1 Dini Group Meg-Array Daughter card Interface

This file describes the Dini Group's standard daughter card interface. The interface provides 186 signals from a host board to a daughter card. These signals are high-speed, flexible and differentially capable.

The daughter card interface is built around a 400-pin FCI "MegArray" connector. This BGA array of pins is designed for high-speed high-density board-to-board connections.

The "Plug" of the system is located on the host, and the "receptacle" is located on the expansion board. This selection was made to give a greater height selection to the daughter card designer.

The user typically designs his own daughter card with interfaces required for the emulation project. The Dini Group is happy to review daughter card designs intended for interface to a Dini Group host for possible compatibility problems. A daughter card designer should use the schematic of the host board (provided with the board) to verify his design.

1.1 Banking System

To allow flexibility to the daughter card designer, the daughter card interface is divided into three "Banks". Each bank can have it's own VCCO power, VREF (threshold voltage) and source-synchronous IO clocking. Each bank contains 62 user IO signals (can be used as 31 differential pairs). Eight of these signals can be used as a source-synchronous clock into the host FPGA. Four of these signals can be used as a reference voltage to the host fpga for standards requiring a reference voltage.

The banks are named B0, B1 and B2, and every user IO on the header interface corresponds to one of these banks. The signals name given to each user IO pin contains either "B0", "B1", or "B2" in the name.

Other connections on the daughter card connector system (not correlated to a bank) include three dedicated, differential clock connections for inputting global clocks from an external source, power connections, bank VCCO power, a buffered power on reset signal.

1.2 Non-Compliant Boards

See section 4.2 of this guide for deviations from this specification.

2 Daughter Card Electrical

The daughter card pin out and routing were designed to allow use of the Virtex-4's 1 Gbps general purpose IO. The connector itself is capable of as high as 10Gbs transmission rates using differential signaling. All signals on the host are all routed as differential, 50-Ohm transmission lines, with means to properly terminate. All signals are routed against a ground plane, so for the best signal integrity, should be routed against a ground plane on the daughter card with excellent

IO voltage bypassing close to the terminus. When signals are used differentially, the trace impedance is 100-ohms.

Signals on the host are not length-matched, except for each signal in a differential pair, which are. Differential pairs are routed in parallel, but not closely coupled to make single-ended signaling possible. Using the IDELAY and ODELAY (Stratix devices adaptive delay) elements on the FPGA, the skew between mismatched signals can be corrected.

Most pins are assigned in a GSG pattern to minimize crosstalk. Some signals are arranged in a GSSG pattern. (Pins in column E and F)

2.1.1 DCI

Host boards whose FPGAs that have DCI (digitally controlled impedance) capabilities have DCI enabled with a 50-ohm reference resistor. This allows LVCMOS_DCI and SSTL_DCI IO standards to be used.

2.2 Daughter card Signals

Bank 0 (VCCO0) includes the signals BL[0-31].
Bank 1 (VCCO1) includes B1L[0-31].
Bank 2 (VCCO2) includes signals B2L[0-31]

Special purpose pins are described below.

2.2.1 Clock Outputs

These signals are used for sending a clock signal (differential) from the daughter card to the host.

The pair GCAP/GCAN (Pairs E1, F1) can be used as a SSTL18, SSTL25, LVDS differential pair, or GCAP can be used single-endedly as LVCMOS25. These signals only connect to the FPGA associated with the connector.

The pair GCBP/GCBN (E3, F3) can be used as a SSTL18, SSTL25, LVDS differential pair, or GCAP can be used single-endedly as LVCMOS25. These signals only connect to the FPGA associated with the connector.

The pair GCCP/GCCN (Pair E5, F5) must be used as an LVDS pair. This differential clock is buffered and distributed to every FPGA on the host. This clock may be de-skewed on the host through a zero-delay buffer. If this is the case (DN7000K10PCI, DN8000K10, DN9000K10PCI) there may be special frequency requirements or settings for the buffers to work. See the user manual for the specific board for these requirements. This clock network may also be multi-purpose, so a setting may have to be used to enable this clock distribution.

2.2.2 User IO

User IO signals connect directly to a general-purpose IO site on the host FPGA. These signals can be used as any drive standard supported by the host FPGA. Each bank must share VCCIO and VREF requirements. For example, if bank B0 is supplied 1.8V by the daughter card on

ALL of the VCCIO_B0 pins, and supplies 0.9V to ALL of the VREF_B0 pins, then the daughter card may use each of the user IO pins as 1.8V SSTL inputs or outputs, LVDS outputs, 1.8V LVCMOS inputs or outputs, since all of these signal standards' requirements are met.

User IO signals can be used single-endedly, or differentially. Differential pairs are pre-selected. Each set of signals whose signal names differ only by a "p" or "n" in the signal name can be used as differential pairs. For example, the signals

B2_L4p and B2_L4n can be used as a differential pair. These two signals are matched in length.

2.2.3 IO Clock

Some of the signals connected to the daughter card expansion headers are "clock-capable"; the inputs on the host FPGA can be used for source-synchronous clocking. On Virtex-4 devices, these pins have "CC" in the name. The CC pins on each bank are suitable for IO, source-synchronous clocking for all signals on that bank. A CC clock can only be used to clock signals on the bank associated with it.

If source-synchronous clocking is not required, these signals can be used as "User IO". On Virtex-4 (DN8000K10 series) the host cannot drive LVDS signals on these pins, due to a hardware constraint.

2.2.4 VREF

Pins declared as "VREF" pins by Xilinx have a defined placement on the daughter card pin out to allow the daughter card to define a logic threshold as required by some standards. If you want to use a standard with a VREF (SSTL15, SSTL15, SSTL18, HSTL15, HSTL18, HSLVCMOS33) the daughter card should supply this reference voltage on these pins. For optimal performance, capacitors should be installed on the host board on these signals near the host's FPGAs. Space provisions for these capacitors have been provided.

If VREF is not required by the intended signaling standard, then these signals can be used as "User IO" without restriction.

2.2.5 Power

The +3.3V, +5.0V and +12V power rails are supplied to the Daughter card headers. Each pin on the MegArray connector is rated to tolerate 1A of current without thermal overload. Most of the power available to daughter cards through the connector comes from the two 12V pins, for a total of 24W. The host provides a fuse on each of these rails.

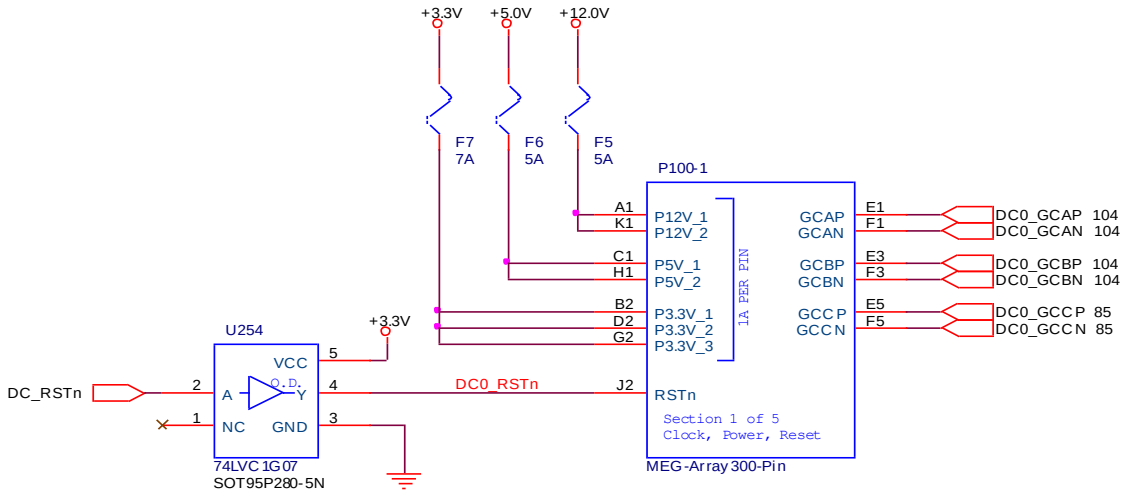
2.2.6 IO Power

The signaling standard of the daughter card is left undefined by the host. For a standard to be used, the daughter card should supply power to the VCCIO pins of the daughter card connector. The pins are connected directly to the VCCIO power pin on the host FPGA. Each of the three banks on the daughter card has two VCCIO pins. Each of the three banks can have its VCCIO set independently, but both pins on a bank must be the same voltage. The daughter card should be able to supply enough current to the host FPGA to power the entire bus. The daughter card designer will need to calculate the host FPGA's current requirements.

When the daughter card does not supply a voltage the host, the host will power these pins at 1.2V with a minimal current capacity. The daughter card can overdrive this voltage safely.

2.2.7 Reset

The reset signal (Active low) is an open-drain, buffered copy of the reset signal on the host. This signal is asserted when the host power is not within tolerance. The signal must be pulled up on the daughter card with a resistor. When the reset signal is active, the FPGAs on the host will not be configured.



The RSTn signal to the daughter card is an open-drain, buffered copy of the SYS_RSTn signal. This signal causes the entire DN8000K10 to reset, losing all FPGA configuration data and resetting the configuration circuitry.

2.3 Pin out

The following lists are the pin assignments to the MEG Array connector. The pins are labeled as in the FCI connector part drawing.

2.3.1 Clock and Reset Signals

F1	GCAP
E1	GCAN
E3	GCBP
F3	GCBN
E5	GCCP
F5	GCCN
J2	RSTn

2.3.2 Power Signals

A1	+12V
K1	+12V
C1	+5V
H1	+5V
B2	+3.3V
D2	+3.3V
G2	+3.3V

2.3.3 Ground Signals

A10	B3	C14	D1	E10	F10	G1	K10	J1	H10
A12	B1	C22	D11	E12	F12	G11	K12	J11	H12
A14	B13	C8	D13	E14	F14	G13	K14	J13	H14
A16	B11	C2	D15	E16	F16	G15	K16	J15	H16
A18	B5	C24	D17	E18	F18	G17	K18	J17	H18
A2	B9	C4	D19	E2	F2	G19	K2	J19	H2
A22	B7	C10	D21	E20	F20	G21	K22	J21	H20
A24	B23	C18	D23	E22	F22	G23	K24	J23	H22
A26	B21	C16	D25	E24	F24	G25	K26	J25	H24
A28	B15	C6	D27	E26	F26	G27	K28	J27	H26
A30	B19	C20	D29	E28	F28	G29	K30	J29	H28
A34	B27	C12	D3	E30	F30	G3	K34	J3	H30
A36	B25	C26	D31	E32	F32	G31	K36	J31	H32
A38	B17	C28	D33	E34	F34	G33	K38	J33	H34
A4	B29	C30	D35	E36	F36	G35	K4	J35	H36
A40	B31	C32	D37	E38	F38	G37	K40	J37	H38
A8	B33	C34	D39	E4	F4	G39	K8	J39	H4
	B35	C36	D5	E40	F40	G5		J5	H40
	B37	C38	D7	E6	F6	G7		J7	H6
	B39	C40	D9	E8	F8	G9		J9	H8

2.3.4 Bank B0 IO

Pins shaded yellow are "CC" pins

A3	DCC0P1	N22
B4	DCC0N1	N23
C3	DCC0P2	H29
D4	DCC0N2	H30
H3	DCC0P3	N27
G4	DCC0N3	P27
K3	DCC0P4	K32
J4	DCC0N4	K33
A5	DCC0P5	M25

B6	DCC0N5_VR	M26
C5	DCC0P6	J27
D6	DCC0N6	K27
H5	DCC0P7	G32
G6	DCC0N7	G33
K5	DCC0P8	M30
J6	DCC0N8_VR	M31
A7	DCC0P9	H32
B8	DCC0N9_VR	J32
C7	DCC0P10	C32
D8	DCC0N10	D32
E7	DCC0P26	J34
F7	DCC0N26	K34
H7	DCC0P11	K28
G8	DCC0N11	K29
K7	DCC0P12	N25
J8	DCC0N12_VR	P26
A9	DCC0P13_C	D34
B10	DCC0N13_C	E34
C9	DCC0P14	H27
D10	DCC0N14	H28
E9	DCC0P27	N29
F9	DCC0N27	N30
H9	DCC0P15	F33
G10	DCC0N15	F34
K9	DCC0P16_C	R22
J10	DCC0N16_C	R23
A11	DCC0P17_C	L30
B12	DCC0N17_C	L31
C11	DCC0P18	L28
D12	DCC0N18	L29
E11	DCC0P28	L33
F11	DCC0N28	L34
H11	DCC0P19	J29
G12	DCC0N19	J30
K11	DCC0P20_C	G30
J12	DCC0N20_C	G31
A13	DCC0P21	P24
B14	DCC0N21	R24
C13	DCC0P22	M27
D14	DCC0N22	M28
E13	DCC0P29	M32
F13	DCC0N29	M33
H13	DCC0P23	P22
G14	DCC0N23	R21
K13	DCC0P24	E32
J14	DCC0N24	E33
A15	DCC0P25	H33

B16	DCC0N25	H34
C15	DCC0P0	P20
D16	DCC0N0	R19
F15	DCC0N30	C34
E15	DCC0P30	C33

2.3.5 Bank B1 IO

Pins shaded yellow are "CC" pins

H15	DCC1P1	B21
G16	DCC1N1	A21
K15	DCC1P2	E28
J16	DCC1N2	F28
A17	DCC1P3	A30
B18	DCC1N3	B30
C17	DCC1P4	K24
D18	DCC1N4	J24
E17	DCC1P26	D24
F17	DCC1N26	D25
H17	DCC1P5	G27
G18	DCC1N5	G28
K17	DCC1P6	D30
J18	DCC1N6	D31
A19	DCC1P7	C29
B20	DCC1N7_VR	C30
C19	DCC1P8	C22
D20	DCC1N8	B22
E19	DCC1P27	D29
F19	DCC1N27	E29
H19	DCC1P9	J25
G20	DCC1N9	K26
K19	DCC1P10	F29
J20	DCC1N10_VR	F30
A21	DCC1P11	G25
B22	DCC1N11_VR	H25
C21	DCC1P12	F25
D22	DCC1N12	F26
E21	DCC1P28	L25
F21	DCC1N28	L26
H21	DCC1P13	B25
G22	DCC1N13	C25
K21	DCC1P14	D27
J22	DCC1N14_VR	E27
A23	DCC1P15_C	A31
B24	DCC1N15_C	B31
C23	DCC1P16	C23

D24	DCC1N16	C24
E23	DCC1P29	B32
F23	DCC1N29	B33
H23	DCC1P17	A28
G24	DCC1N17	A29
K23	DCC1P18_C	B28
J24	DCC1N18_C	C28
A25	DCC1P19_C	B27
B26	DCC1N19_C	C27
C25	DCC1P20	B23
D26	DCC1N20	A23
E25	DCC1P30	E31
F25	DCC1N30	F31
H25	DCC1P21	D26
G26	DCC1N21	E26
K25	DCC1P22_C	F23
J26	DCC1N22_C	E23
A27	DCC1P23	A26
B28	DCC1N23	B26
C27	DCC1P24	A24
D28	DCC1N24	A25
H27	DCC1P25	G23
G28	DCC1N25	H24
K27	DCC1P0	F24
J28	DCC1N0	E24

2.3.6 Bank B2 IO

Pins shaded yellow are "CC" pins

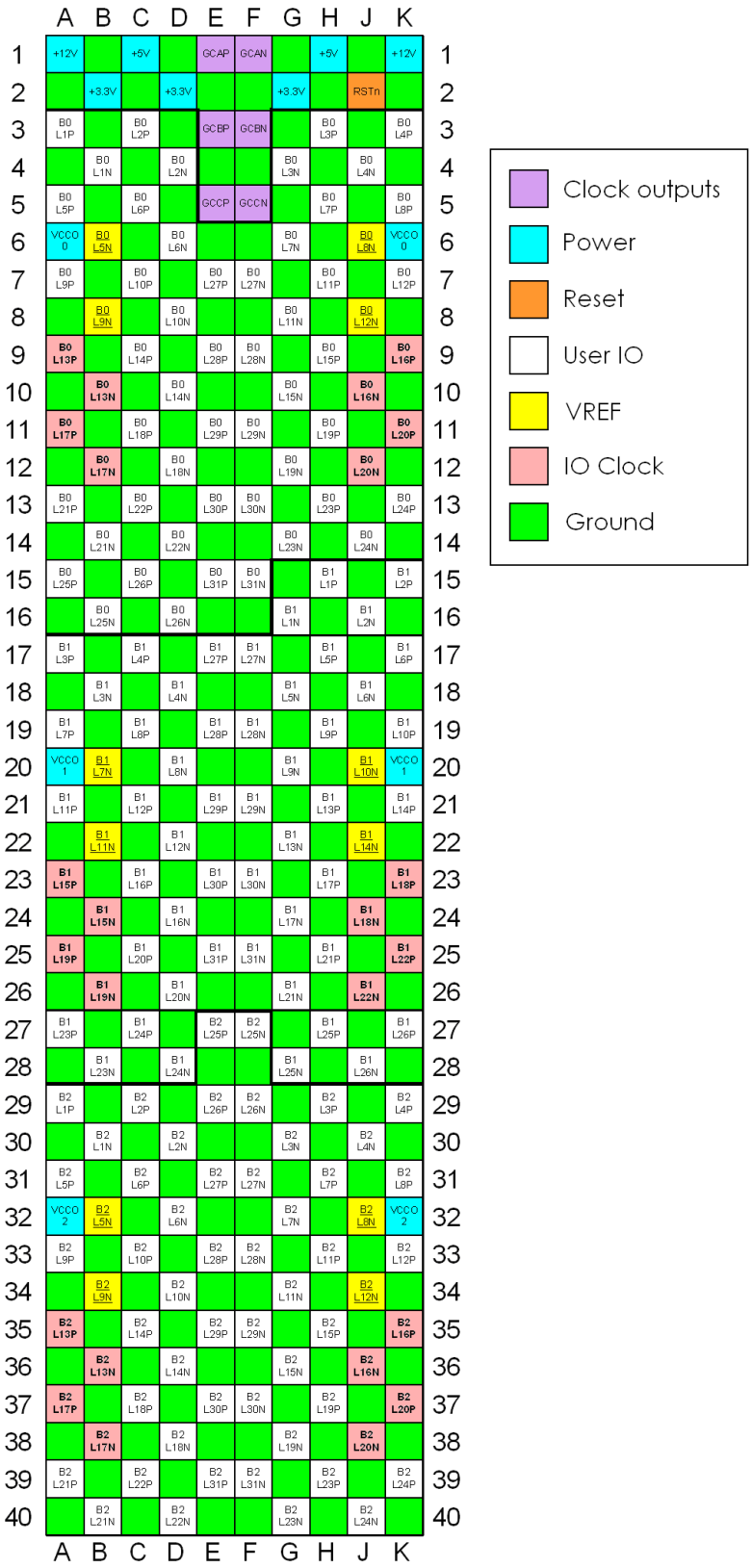
E27	DCC2P28	N32
F27	DCC2N28	P32
A29	DCC2P30	P30
B30	DCC2N30	P31
C29	DCC2P2	T24
D30	DCC2N2	T25
E29	DCC2P29	AB31
F29	DCC2N29	AA31
H29	DCC2P3	Y29
G30	DCC2N3	W29
K29	DCC2P4	W27
J30	DCC2N4	V27
A31	DCC2P5	R27
B32	DCC2N5_VR	R28
C31	DCC2P6	T23
D32	DCC2N6	U23
E31	DCC2P25	P29

F31	DCC2N25	R29
H31	DCC2P7	U30
G32	DCC2N7	U31
K31	DCC2P8	Y31
J32	DCC2N8_VR	W31
A33	DCC2P9	V28
B34	DCC2N9_VR	V29
C33	DCC2P10	W32
D34	DCC2N10	V32
E33	DCC2P26	AB32
F33	DCC2N26	AB33
H33	DCC2P11	U26
G34	DCC2N11	U27
K33	DCC2P12	T28
J34	DCC2N12_VR	U28
A35	DCC2P13_C	N33
B36	DCC2N13_C	N34
C35	DCC2P14	V23
D36	DCC2N14	V24
E35	DCC2P27	AA33
F35	DCC2N27	AA34
H35	DCC2P15	T33
G36	DCC2N15	T34
K35	DCC2P16_C	Y32
J36	DCC2N16_C	Y33
A37	DCC2P17_C	W30
B38	DCC2N17_C	V30
C37	DCC2P18	V33
D38	DCC2N18	V34
E37	DCC2P1	R26
F37	DCC2N1	T26
H37	DCC2P19	R31
G38	DCC2N19	T31
K37	DCC2P20_C	P34
J38	DCC2N20_C	R34
A39	DCC2P21	U32
B40	DCC2N21	U33
C39	DCC2P22	V25
D40	DCC2N22	U25
E39	DCC2P0	Y27
F39	DCC2N0	Y28
H39	DCC2P23	T29
G40	DCC2N23	T30
K39	DCC2P24	R32
J40	DCC2N24	R33

2.3.7 VCCIO Signals

VCCO corresponds to bank B0, VCC1 corresponds to bank B1, VCC2 corresponds to bank B2.

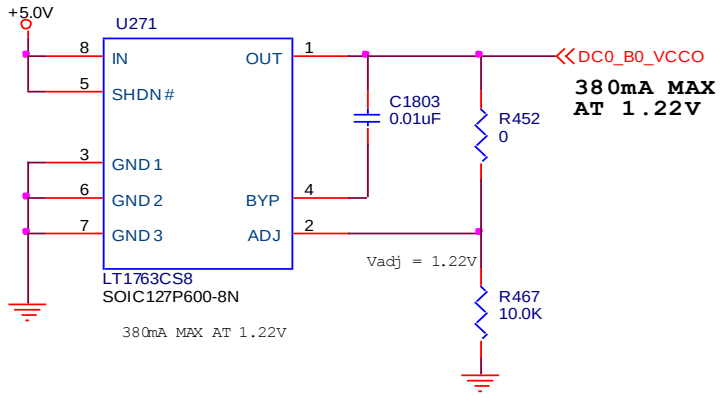
K6	VCCO0
A6	VCCO0
K20	VCCO1
A20	VCCO1
A32	VCCO2
K32	VCCO2


A B C D E F G H J K
1 +12V +5V GCAP GCAN +5V +12V
2 +3.3V +3.3V +3.3V RSTn
3 B0 L1P B0 L2P GCBP GCBN B0 L3P B0 L4P
4 B0 L1N B0 L2N B0 L3N B0 L4N
5 B0 L5P B0 L6P GCCP GCCN B0 L7P B0 L8P
6 VCCO 0 B0 L5N B0 L6N B0 L7N B0 L8N VCCO 0
7 B0 L9P B0 L10P B0 L27P B0 L27N B0 L11P B0 L12P
8 B0 L9N B0 L10N B0 L11N B0 L12N
9 B0 L13P B0 L14P B0 L28P B0 L28N B0 L15P B0 L16P
10 B0 L13N B0 L14N B0 L15N B0 L16N
11 B0 L17P B0 L18P B0 L29P B0 L29N B0 L19P B0 L20P
12 B0 L17N B0 L18N B0 L19N B0 L20N
13 B0 L21P B0 L22P B0 L30P B0 L30N B0 L23P B0 L24P
14 B0 L21N B0 L22N B0 L23N B0 L24N
15 B0 L25P B0 L26P B0 L31P B0 L31N B1 L1P B1 L2P
16 B0 L25N B0 L26N B1 L1N B1 L2N
17 B1 L3P B1 L4P B1 L27P B1 L27N B1 L5P B1 L6P
18 B1 L3N B1 L4N B1 L5N B1 L6N
19 B1 L7P B1 L8P B1 L28P B1 L28N B1 L9P B1 L10P
20 VCCO 1 B1 L7N B1 L8N B1 L9N B1 L10N VCCO 1
21 B1 L11P B1 L12P B1 L29P B1 L29N B1 L13P B1 L14P
22 B1 L11N B1 L12N B1 L13N B1 L14N
23 B1 L15P B1 L16P B1 L30P B1 L30N B1 L17P B1 L18P
24 B1 L15N B1 L16N B1 L17N B1 L18N
25 B1 L19P B1 L20P B1 L31P B1 L31N B1 L21P B1 L22P
26 B1 L19N B1 L20N B1 L21N B1 L22N
27 B1 L23P B1 L24P B2 L25P B2 L25N B1 L25P B1 L26P
28 B1 L23N B1 L24N B1 L25N B1 L26N
29 B2 L1P B2 L2P B2 L26P B2 L26N B2 L3P B2 L4P
30 B2 L1N B2 L2N B2 L3N B2 L4N
31 B2 L5P B2 L6P B2 L27P B2 L27N B2 L7P B2 L8P
32 VCCO 2 B2 L5N B2 L6N B2 L7N B2 L8N VCCO 2
33 B2 L9P B2 L10P B2 L28P B2 L28N B2 L11P B2 L12P
34 B2 L9N B2 L10N B2 L11N B2 L12N
35 B2 L13P B2 L14P B2 L29P B2 L29N B2 L15P B2 L16P
36 B2 L13N B2 L14N B2 L15N B2 L16N
37 B2 L17P B2 L18P B2 L30P B2 L30N B2 L19P B2 L20P
38 B2 L17N B2 L18N B2 L19N B2 L20N
39 B2 L21P B2 L22P B2 L31P B2 L31N B2 L23P B2 L24P
40 B2 L21N B2 L22N B2 L23N B2 L24N
A B C D E F G H J K
Clock outputs
Power
Reset
User IO
VREF
IO Clock
Ground

2.4 VCCO bias generation

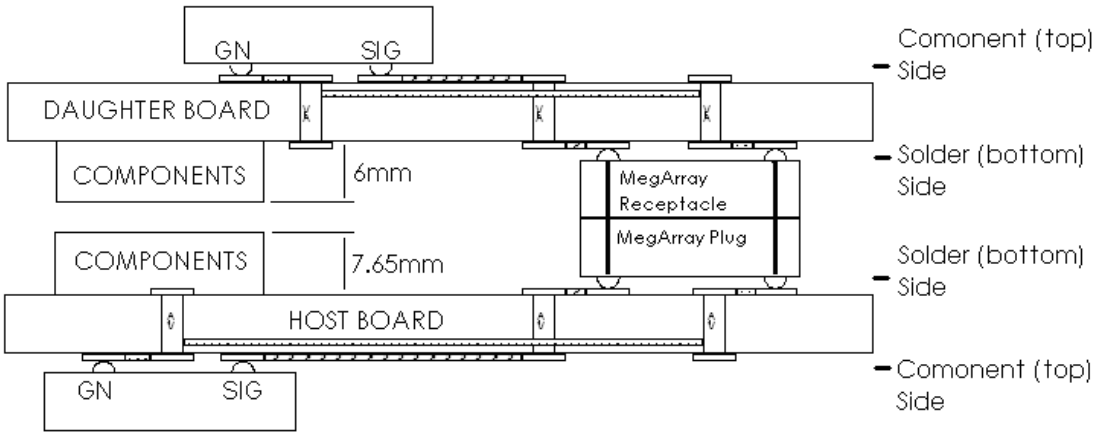
Since a daughter card will not always be present on a daughter card connector, a VCCO bias generator is used on the motherboard for each daughter card bank to keep the VCCO pin on the FPGA within its recommended operating range. The VCCO bias generators supply +1.2V to the VCCO pins on the FPGAs, and are back-biased by the daughter card when it drives the VCCO rails.

The VCCO voltage impressed by the daughter card should be less than 3.75 to prevent destruction of the Virtex 4 IOs connected to that daughter card.



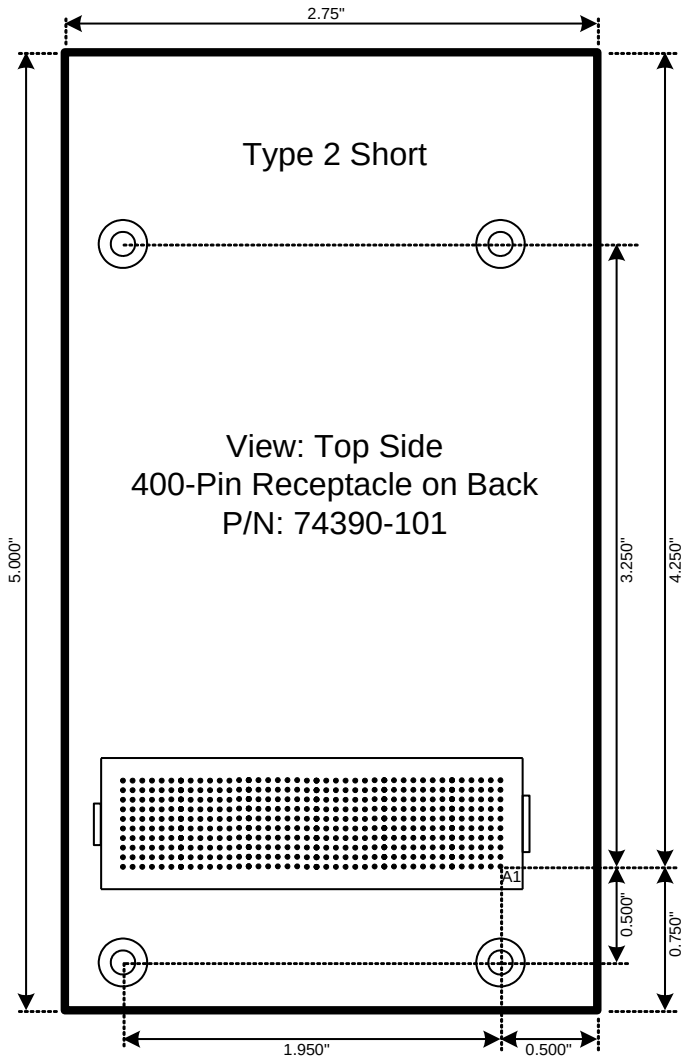
3 Daughter card Mechanical

Daughter card expansion headers are located on the bottom side of the PWB. This is done to eliminate the need for resolving board-to-board clearance issues, assuming the daughter card uses no large components on the backside.



Each host with a daughter card interface makes certain minimal provisions for daughter cards. Enough space is reserved for each daughter card plug to accommodate the following hypothetical daughter card. (The DNMEG_OBS400 conforms to these dimensions)

Note that the components on the topside of the daughter card and DN8000K10 face in opposite directions.



At least four mounting positions are provided for each header in a standard location, as shown above.

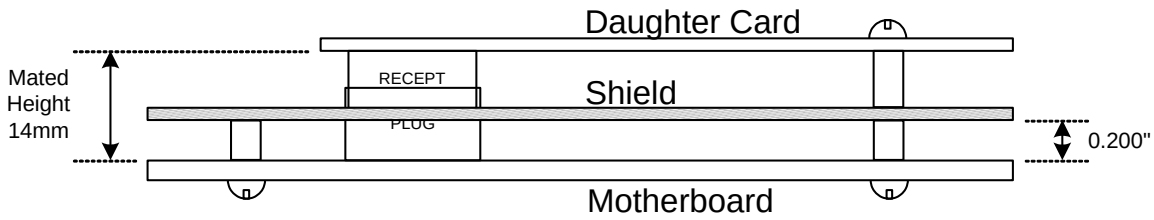
Boards that have multiple daughter card connectors next to each other (horizontally) use a standard spacing of 78.25mm (3.08in) from pin A1 to pin A1. (and aligned vertically)

The connectors used in the expansion system on the host are FCI MEG-Array 400-pin plug, 6mm, part #84520-102. A suitable mating connector for use on a daughter card would be FCI

part 74390-101 (lead-free 74390-101LF). This provides the minimum board-to-board spacing. Other spacings are possible with different connectors on the daughter card.

3.1.1 Daughter card mounting DN8000K10

The DN8000K10 features a standard metal base plate that gives the board mechanical stability, and provides plenty of mounting points for daughter cards. The daughter card receptacle on the daughter card itself will also be mounted on the backside of the board.



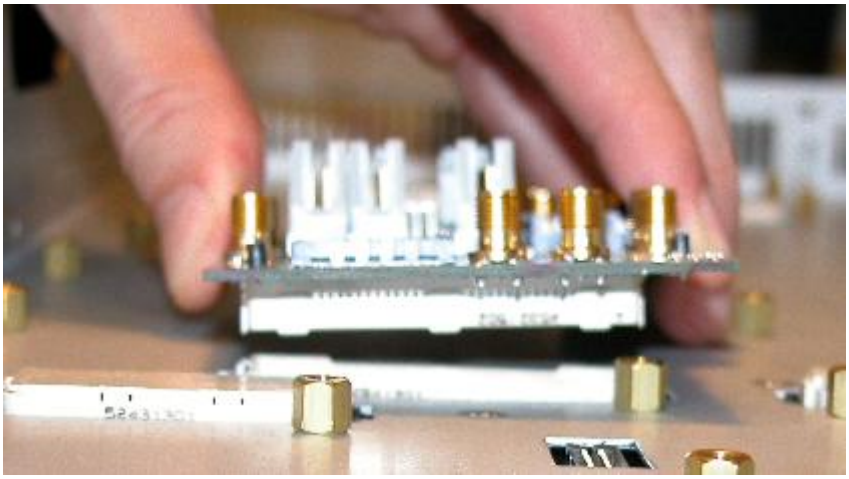
The daughter card should use standoffs to secure itself to the backside of the base plate. The standard chassis that comes with the DN8000K10 will allow it to operate FPGA side down, or on its side to allow physical access to the daughter card and the controls of the DN8000K10.

With this host-plate-daughter card arrangement, there is a limited Z dimension clearance for backside components on the daughter card. This dimension is determined by the daughter card designer's part selection for the MegArray receptacle.

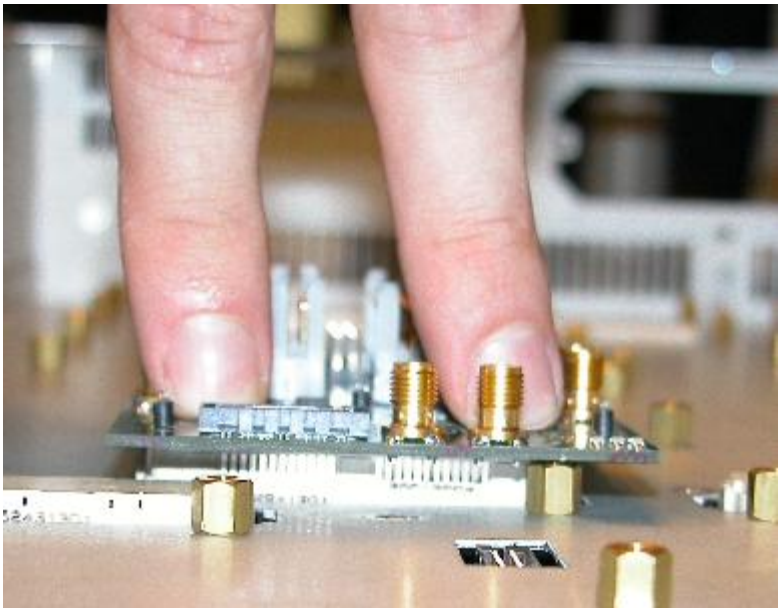
3.1.2 Insertion and removal

Due to the small dimensions of the very high speed MegArray connector system, the pins on the plug and receptacle of the Meg Array connectors are very delicate.

When plugging in a daughter card, make sure to align the daughter card first before pressing on the connector. *Be absolutely certain that both the small and the large keys at the narrow ends of the Meg Array line up BEFORE applying pressure to mate the connectors!*



Place it down flat, then press down gently.



The following two excerpts are taken from the FCI application guide for the Meg Array series of connectors.

A part can be started from either end. Locate and match the connector's A1 position marking ("?") for both the Plug and Receptacle. (Markings are located on the long side of the housing.) Rough alignment is required prior to connector mating as misalignment of >0.8mm could damage connector contacts. Rough alignment of the connector is achieved through matching the Small alignment slot of the plug housing with the Small alignment key of the receptacle housing and the Large alignment slot with the Large alignment key. Both connector housings have generous lead-in around the perimeter and will allow the user to blind mate assemble the connectors. Align the two connectors by feel and when the receptacle keys start into the plug slots, push down on one end and then move force forward until the receptacle cover flange bottoms on the front face of the plug.
Dec 09, 2004

Like mating, a connector pair can be unmated by pulling them straight apart. However, it requires less effort to un-mate if the force is originated from one of the slot/key ends of the assembly. (Reverse procedure from mating) Mating or un-mating of the connector by rolling in a direction perpendicular to alignment slots/keys may cause damage to the terminal contacts and is not recommended.

4 Dini Group products

4.1 Board List

The following boards comply with this document's header specifications:

DN7000K10PCI	3 Headers
DN8000K10	11 Headers (7 are non-standard)
DN8000K10PSX	1 Header
DNMEG_S2GX	1 Header

Coming Soon:

DN9000K10PCI	3 Headers
DNMEG_ADC	1 Header

4.2 Exceptions

The following products have headers that do not fully comply with these specification. A list of exceptions to this specification follows, with a description of the deviation.

4.2.1 DN8000K10PSX

GCCP/GCCN is not deskewed on the host. FPGAs on the host will receive this signal synchronized with respect to each other, but with no phase relationship with the daughter card.

4.2.2 DN8000K10

Daughter cards D0, D1, D2, D3, D4, D9 use 300-pin Meg Array connectors instead of 400-pin. The signal definitions remain the same, except that pin rows 29-40 are not present, and the connector supports two banks (B0, B1) instead of three.

DC0 and DC3 do not comply with these specifications. See the DN8000K10 user guide and schematic. (These headers are used for RocketIO signaling) These signals are routed as 110-ohm differential pairs, instead of 100-Ohm.

DC10 is reserved for Dini Group use and should not be used for a custom daughter card without the cooperation of Dini Group.

4.2.3 DN7000K10PCI

Banks B0 and B1 must be set to the same VCCIO voltage. These two nets are connected on the host.

4.2.4 DNMEG_S2GX

Note that only DC_TOP (P4) is a daughter card header that complies with this specification. P5 is the receptacle for a host board.

4.2.5 DN9000K10

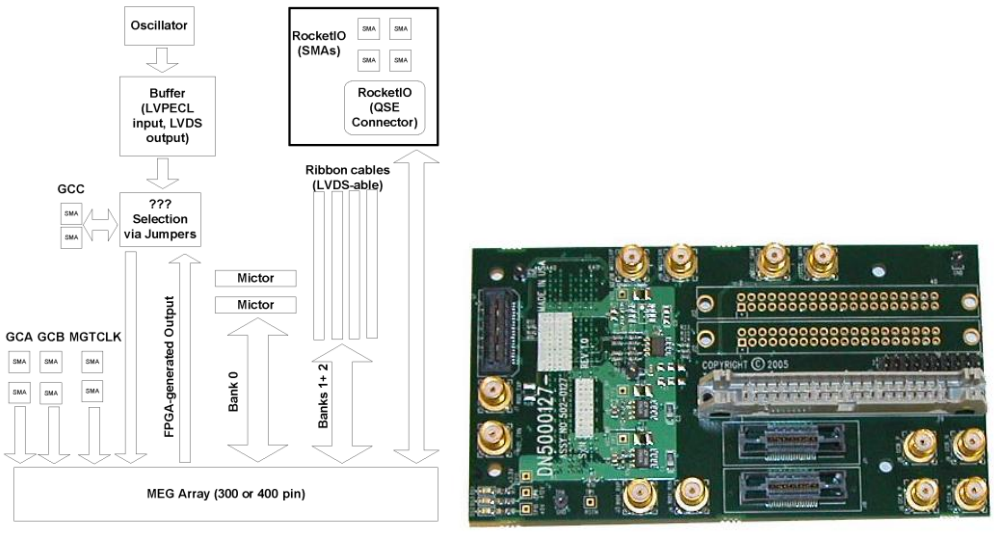
On headers DC4 and DC9, VCCO is shared between some banks. See the User Manual for a complete description of this deviation.

4.3 Standard Daughter cards

The Dini Group has some general-purpose daughter cards available. See the Dini Group website for more information.

4.3.1 DNMEG_OBS400

The breakout daughter card provides 48 signals on Mictor connector, 124 signals on .1" pitch headers arranged for differential signaling, 14 differential coax cable connection (intended for use with the DN8000K10 rocketIO headers) and global clock inputs.



4.3.2 DNMEG_OBS300

The DNMEG_OBS300 is identical to the DNMEG_OBS400 except that the receptacle is a 300-pin instead of a 400-pin connector. This can only be used with DC0, DC1, DC2, DC3, DC4, DC9 on the DN8000K10.

4.3.3 DNMEG_S2GX

This board provides a Stratix 2 GX FPGA, capable of 6.5Gbs serial data transmission. And some memory options.

The DNMEG_S2GX also has a daughter card header configured as a pass-through from it's own daughter card receptacle.

4.3.4 DNMEG_ADC (coming soon)

This board provides a high-speed ADC and DAC, 1Gb Ethernet, Virtex-4 SX55 FGPA, and Memory options.

4.3.5 DNMEG_DVI (coming soon)

This board provides dual DVI-D input and output and memory options.

4.3.6 DNMEG_ARM (coming soon)

Arm processor

4.3.7 DNMEG_PROTO (coming soon)

Prototype area